What is claimed is:

1. A method for fabricating a device having a substrate, a contact plug through the substrate, a first barrier layer on said substrate, a first electrode on said first barrier layer, a dielectric layer on said first electrode, and a second electrode on said dielectric layer, the method comprising the steps of:

forming a first hardmask over the second electrode;

etching said second electrode and said dielectric layer of said device, using said first hardmask to shape said second electrode and said dielectric layer;

removing said first hardmask;

applying one or more encapsulating layers to said second electrode and said dielectric layer;

applying a second hardmask to said one or more encapsulating layers;

etching said first electrode according to said second hardmask down to said first barrier layer; and

removing said second hardmask from said one or more encapsulating layers.

2. The method of claim 1, further comprising etching said first barrier layer through to said substrate after the step of removing said second hardmask from one or more encapsulating layers.

3. The method of claim 2, further comprising applying one or more cover layers to said devices after the step of etching said first barrier layer.

4. The method of claim 1, further comprising annealing said device after the step of removing said first hardmask.

5. The method of claim 1, wherein the step of removing said first hardmask comprises applying a dry etching process.

6. The method of claim 1, wherein the step of removing said first hardmask comprises applying a dry etching process having a high etching selectivity of said interlayer dielectric layer relative to said first and/or said second electrode.

7. The method of claim 1, wherein the step of forming a dielectric layer on said first electrode comprises forming a ferroelectric layer on said first electrode.

8. The method of claim 1, wherein the step of etching said second electrode and said dielectric layer comprises etching said second electrode and said dielectric layer to divide the device into a number of devices having a common first electrode.

9. A device comprising:

a substrate;

a contact plug passing through said substrate;

a first barrier layer formed on said substrate;

a first electrode formed on said first barrier layer;

a dielectric layer formed on said first electrode;

a second electrode formed on said ferroelectric layer;

a first encapsulation layer formed directly on said second electrode;

one or more further encapsulation layers formed directly on said first encapsulation layer, said one or more further encapsulation layers extending to said first electrode to protect side faces of said dielectric layer;

one or more cover layers formed on said one or more further encapsulation layers.

10. The device of claim 9, wherein said first barrier layer is an electrically conducting layer.

11. The device of claim 9, further comprising one or more further barrier layers on said first barrier layer.

12. The device of claim 9, wherein said dielectric layer is formed of a ferroelectric material.

13. The device of claim 9, wherein said dielectric layer is formed of PZT.

14. The device of claim 9, further comprising one or more oxide electrode layers between said first electrode and said dielectric layer.

15. The device of claim 14, wherein said one or more oxide electrode layers comprise $SrRuO_3$.

16. The device of claim 9, wherein said one or more cover layers extend to said substrate.

17. A ferroelectric capacitor device comprising the device of claim 9.

18. A device formed according to the method of claim 1.

19. A Random Access Memory device comprising one or more devices according to claim 9.